FAIRCHILD

MEMORY PRODUCTS

MOUNTAIN VIEW, CALIFORNIA

MP MASTER
MA30047

TECHNICAL MANUAL

MicroCELL™ MEMORY SYSTEM
128 Words x 24 Bits/Word
FAIRCHILD MEMORY PRODUCTS
Mountain View, California

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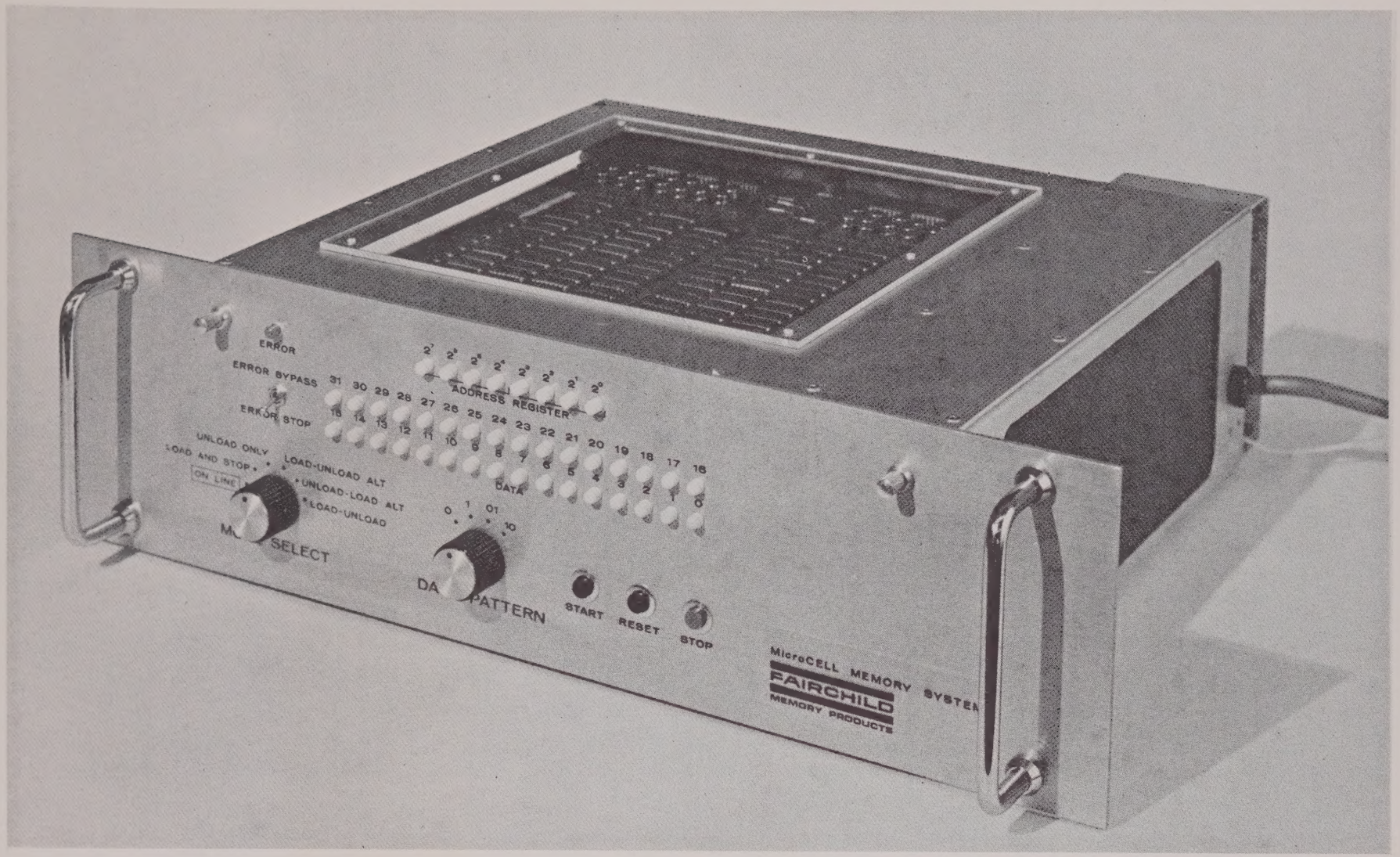
MEMORY PRODUCTS



256 x 32 Maximum

TABLE OF CONTENTS

Section			Page
I	GENERAL INFORMATION		
	1-1	Introduction	1-1
	1-2	Description	1-1
	1-3	Electrical Specifications	1-2
	1-4	Mechanical Specifications	1-2
II	THEORY OF OPERATION		
	2-1	Introduction	2-1
	2-2	General System Organization	2-1
III	OPERATIONAL INFORMATION		
	3-1	Introduction	3-1
	3-2	Installation	3-1
	3-3	MicroCELL Logic	3-2
	3-4	MicroCELL Assembly	3-3
	3-5	MicroCELL Operation	3-4
IV	MAINTENANCE PROCEDURES		
	4-1	Introduction	4-1
	4-2	Maintenance	4-1
V	POWER SUPPLY		
	5-1	Introduction	5-1
	5-2	Description	5-1
VI	MISCELLANEOUS INFORMATION		
	6-1	Introduction	6-1
	6-2	Cannon Connector Information	6-1
	6-3	Off Line Operation	6-1
		Accessories List	6-3
	LIST OF DRAWINGS		iii
	LIST OF ILLUSTRATIONS		ii
	LIST OF TABLES		i

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LIST OF ILLUSTRATIONS

Figure		Page
1-1	Interface Timing Diagram	1-5
2-1	General Block Diagram	2-3
2-2	Storage Array Organization	2-4
2-3	Complete Memory Cycle - Word Line and Bit Line Waveforms	2-5
3-1	Details of Power Cable	3-6
3-2	One Bit of 16 Bit Storage Device	3-7
3-3	Word Driver Plus Second Level Decoder . .	3-8
3-4	Interface Connector Chart	3-9
3-5	Data Storage Board Voltage Check Points. .	3-11
6-1	Component Pin Diagram (Top View)	6-7

LIST OF TABLES

Table		Page
1-1	Electrical Specifications	1-3
1-2	Mechanical Specifications	1-4
3-1	Signals and Their Description	3-10
4-1	Error List	4-2
6-1	Exerciser Operational Mode Capabilities. .	6-4
6-2	Test Capability of the Exerciser	6-5

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LIST OF DRAWINGS

MicroCELL MEMORY SYSTEM

[illegible]	Memory Control Logic
[illegible]	Memory Control Assembly
[illegible]	Bit Driver Logic
[illegible]	Bit Driver Assembly
[illegible]	Data Storage Logic
[illegible]	Data Storage Assembly
[illegible]	Negative TTμL Interface Logic
[illegible]	Negative TTμL Output Interface Assembly
[illegible]	Internal Exerciser Logic
[illegible]	Internal Exerciser Assembly
[illegible]	Exerciser Panel Assembly
[illegible]	Wiring Diagram (Exerciser)
[illegible]	Exerciser Test Cable
[illegible]	Power Cable Assembly
[illegible]	MicroCELL Memory System Assembly
[illegible]	Wiring List

MicroCELL POWER SUPPLY

PR56-C1-1	Installation, Scratchpad Memory
PR56-C1-2	Circuit Diagram PR56-C1
480-2484	Circuit Diagram Logic and Pass
480-2485	Circuit Diagram Pass Board +5, +2
480-2486	Circuit Diagram Regulated

SECTION I

GENERAL INFORMATION

1-1 INTRODUCTION

This manual provides information for operation and maintenance of the MicroCELL Memory System and the associated power supply. This Section (Section I) contains general information, a system description, and system specification. Section II presents the theory of operation of the memory and Section III provides operational information. Section IV outlines maintenance procedures to allow error free operation, and Section V provides a description of the power supply. Section VI presents miscellaneous information including accessories list and wiring list.

1-2 DESCRIPTION

The MicroCELL Memory System is a high-speed, random access storage system, that accomplishes the storage function by utilizing bipolar integrated circuit flip-flops. The high-speed feature allows repetitive addressing of the memory at 135 nanoseconds (cycle time) as well as receipt of data from memory 135 nanoseconds after the command (access time). The random access feature allows equal cycle time and access times for all addresses in memory.

Parallel entry of address, command, and data is required, and data is delivered from memory in parallel form.

Two properties of the MicroCELL Memory, namely, non-destructive read-out (NDRO) and direct coupling throughout, offer certain advantages. The NDRO property allows continuous loading of data into memory at the 135 nanosecond cycle time or continuous unloading of data from memory at the same 135 nanosecond rate. The DC coupling feature obviates the need for a register to store output data, since the data is available for the entire cycle.

In addition to continuous load or continuous unload of data, a continuous unload-load rate of 135 nanoseconds can be achieved.

1-3 Electrical Specifications

Table 1-1 lists electrical specifications for the MicroCELL Memory System.

1-4 Mechanical Specifications

Table 1-2 lists mechanical specifications for the MicroCELL Memory System including the power supply.

TABLE 1-1 ELECTRICAL SPECIFICATIONS

Capacity:	128 words, 24 bits/word
Address Inputs:	Single Rail, 7 bits (7 lines), TTμL levels
Data Inputs:	Single Rail, 24 lines, TTμL levels
Data Outputs:	Single Rail, 24 lines, TTμL levels
Commands:	Load (Write) 1 line, TTμL level Unload (Read) 1 line, TTμL level
Internal Logic Levels:	Binary "0" = - 0.5V ± 0.5V Binary "1" = - 2.5V ± 0.5V
Interface:	Input: Direct input to μA710C Output: TTμL 9009, 62Ω series termination
Modes of Operation:	Load (Write) Unload (Read)
Cycle Time:	DC to 135 nanoseconds
Access Time:	135 nanoseconds
Pulse Widths:	Load: 35 nanoseconds minimum, mid-point to mid-point. Unload: 35 nanoseconds minimum, mid-point to mid-point. Address Inputs: 60 nanoseconds minimum, cycle time maximum. Data Inputs: 80 nanoseconds minimum, 40 nanoseconds delay from LOAD to 120 nanosecond delay from LOAD.
Data Outputs:	Equal to cycle time.
Pulse Delays:	See Figure 1-1 Interface Timing Diagram
Power Requirements:	Power Supply

Nominal Voltage	Static Regulation	Full Load Current	Power Supply Current Capability
+13 V	±3%	.600A	1.0A
+ 5 V	±3%	12A	21.0A
+ 2 V	±5%	2A	9.2A
- 1.6V	±5%	.150A	1.6A
- 2 V	±5%	4A	8.0A
- 5 V	±3%	6A	20.0A

Temperature Range: (At Nominal Voltages)	10°C to 55°C.

Table 1-2 MECHANICAL SPECIFICATIONS

		Memory	Power Supply
Dimensions:	Width	14"	17"
	Depth	16" (including mating connector)	16"
	Height	5.25"	5/25"
	Weight	25 lbs	70 lbs
Mounting:	Both memory and power supply have 19" wide front panels, equipped for rack mounting.		
Slides:	The memory is equipped with slides which allow it to be pulled out in front of the rack. (Refer to Chassis-Trac, Inc., Indianapolis, Indiana, Dwg. #C-300-S for further details).		
Cooling:	The MicroCELL is cooled by two Rotron fans. The cord from the rear of the MicroCELL provides input power to the fans. Fans should always be ON before memory operation commences.		

ns
0
50
100
135
150
200
Optional
Optional
Optional
Optional
Optional
Optional
Optional
Cycle time
Optional
Optional
Optional
Optional
Optional
Optional
Optional

SECTION II

THEORY OF OPERATION

2-1 Introduction

This section describes the general operational theory of the MicroCELL Memory System.

2-2 General System Organization

The general organization of the MicroCELL Memory System is shown in the block diagram of Figure 2-1. The seven primary functions, ADDRESS REGISTER, FIRST LEVEL DECODER, SECOND LEVEL DECODER PLUS WORD DRIVERS, STORAGE, BIT DRIVERS, SENSE AMPLIFIERS PLUS DATA BUFFERS, and TIMING AND CONTROL.

The MicroCELL memory is a 2-wire, word organized system. The 2-wire characteristic refers to the fact that for any one storage location only 2 lines are required; a word line and a common bit-sense line. Word organized refers to the way in which the storage is selected; that is, one word driver selects all storage bits of one address. Both these features are illustrated in the block diagram of Figure 2-2, which shows the interconnections of word drivers, bit drivers and sense amplifiers to the storage locations. The dashed lines represent the physical integrated circuit (IC) packages.

The basic storage device is a 16-bit bipolar IC in a 16-lead Dual In-line Package (DIP). The device is organized in a 4 word by 4 bit array as shown in Figure 2-2. The total memory system is obtained by adding the desired number of basic storage devices in both the X and Y direction along with the appropriate number of word drivers, bit drivers and sense amplifiers.

The detailed operation of each of the functional blocks of Figure 2-1 is described in SECTION III. However, the general operation of the storage, word drivers, bit drivers and sense amplifiers will be described here. See Figure 2-3.

The waveforms shown in Figure 2-3 comprise the complete group of operations performed on a bit of storage: write binary zero (W"0"), read binary zero (R"0"), wire binary one (W"1"), and read binary one (R"1").

To perform the W"0" operation, a positive polarity pulse appears on the desired word line (1 out of the total number) while simultaneously a negative polarity pulse appears on the bit lines which will store zeros. To determine if the appropriate bits have stored the zero, a R"0" operation can be initiated. This is accomplished by driving the same word line with a positive polarity pulse of a smaller amplitude and sensing the readouts on the common bit-sense lines. A low readout on the appropriate lines as shown in the waveform corresponds to a zero.

The W"1" operation is similar to the W"0" except the bit line remains at its standby level. By initiating the R"1" operation (same waveform as R"0" on the word line) a positive readout will be sensed on the common bit-sense lines.

Under normal memory operation, any and all combinations will appear simultaneously in the bits of the same word. This is controlled simply by the input data levels.

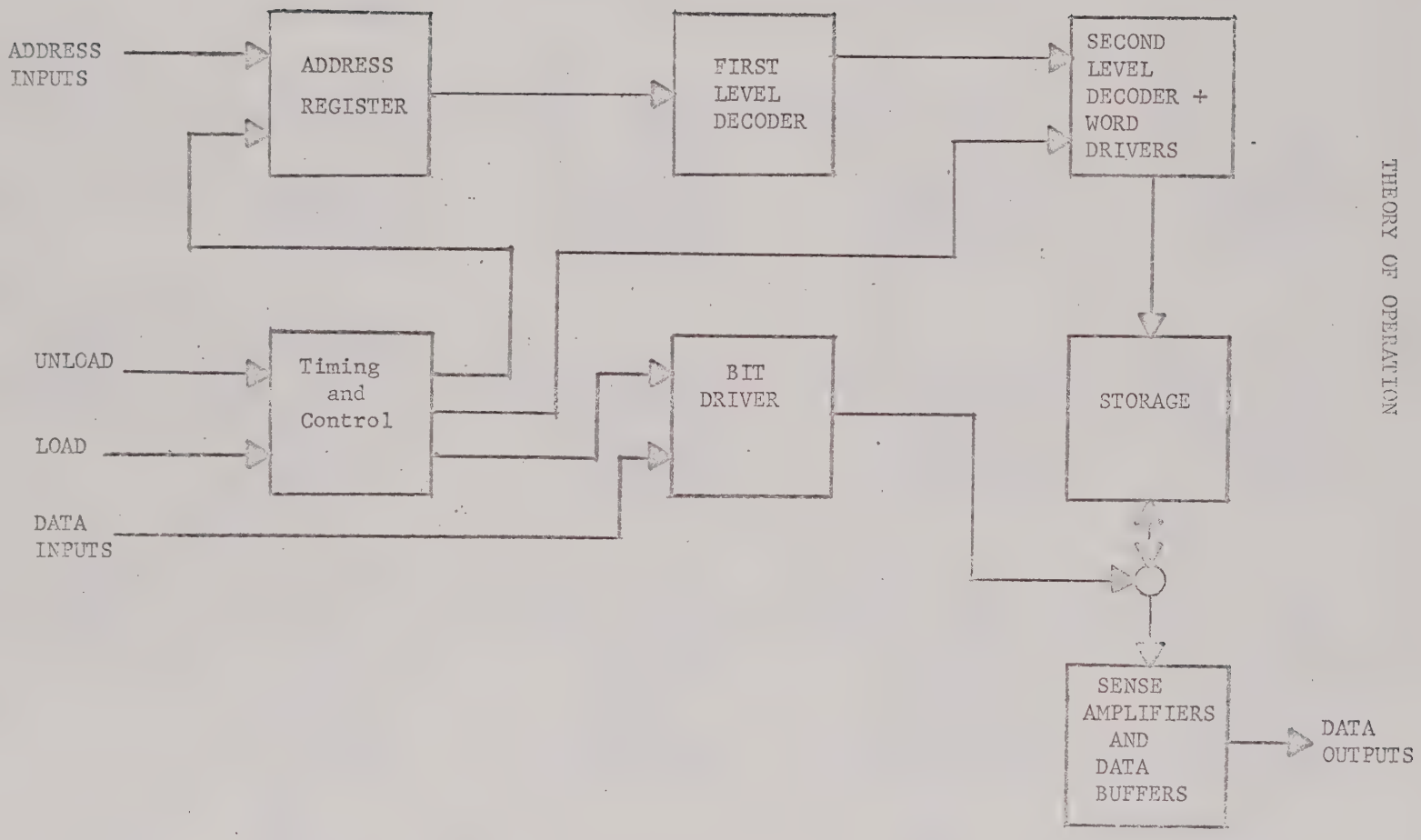

FIGURE 2-1 GENERAL BLOCK DIAGRAM

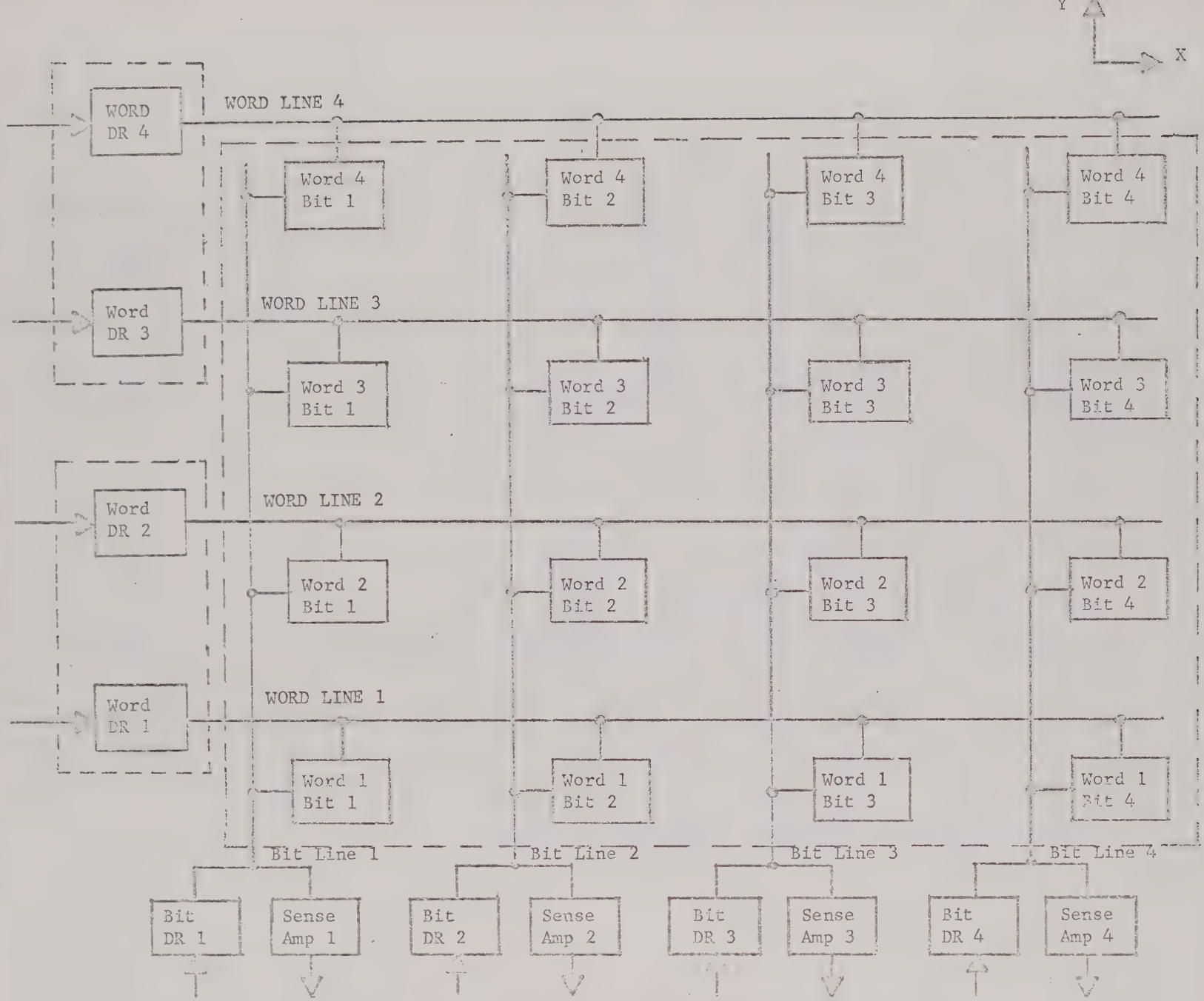

Figure 2-2 Storage Array Organization

Figure 2-3 Complete Memory Cycle - Word Line and Bit Line Waveforms

SECTION III

OPERATIONAL INFORMATION

3-1 Introduction

This section covers the following topics: installation, details of memory logic, assembly and operation.

3-2 Installation

Installation of the MicroCELL Memory System commences with the connection of the memory to the power supply by the use of the 50-wire, color-coded, power cable harness. Details of the power cable are given in Figure 3-1. The details include the color-code designation, the wiring diagram to the Amphenol Connector and the physical characteristics of the power cable. The Amphenol Connector mates with the bottom Amphenol Connector, designated J11, on the back of the MicroCELL. The lugs on the opposite end of the power cable are placed on the designated positions on the terminal block of the power supply. See MicroCELL Memory System Assembly and Power Supply Installation Drawing for further details.

The power supply is capable of delivering the full load current values to the six voltages as shown in Table 1-1. For proper power supply operation, the input power cord, designated on Power Supply Installation Drawing, must be connected to 115 VAC, 60 Hz, single phase. The ON-OFF switch, designated S1 on the Power Supply Installation Drawing, is located on the power supply front panel.

For proper memory operation, the following procedure should be used.

1. Remove top cover plate of the MicroCELL.

2. See panel for appropriately marked voltages. Exception: the -1.6v is adjusted to the value on the system voltage tag.

3. Adjust correct nominal voltages according to Table 1-1, starting with -5V, by setting potentiometers as marked on back panel of the power supply.

4. Measure voltages at the top (the filter capacitor end) of the first printed circuit board. See Figure 3-5.

5. All values of voltage can be measured and set on this board with the exception of the -1.6 adjustable.

6. The -1.6 adjustable can be measured on the pin of the Cannon connector; connector position J-5, pin numbers A21 and B8. This voltage should be set to the value marked on the memory system voltage tag.

7. After setting -5V, the other five voltages can be set in any order.

8. To achieve proper memory operation at the nominal voltages, apply interface signals in accordance with the Interface Timing Diagram of Figure 1-1, to the appropriate pins of the Amphenol connectors shown on the Wiring Lists and Figure 3-4, Interface Connector Diagram. Specifically, the ADDRESS INPUTS are designated as EAI1 through EAI7 under Signals on the Wiring List. The DATA INPUTS are designated as EDI1 through EDI24, and DATA OUTPUTS are DO1 through DO24. LOAD is designated as ELD, UNLOAD is designated as EUL.

9. Printed circuit board positions in the package, from the bottom to the top are: Interface (or exerciser) in A7, Memory Control in A6, Bit Driver in A5, Data Storage in A1 & 3.

3-3 MicroCELL Logic

The MicroCELL detailed logic is summarized on three drawings (grouped by physical assembly). Referring to the general block diagram of Figure 2-1, the blocks are related to the three logic drawings as follows:

The three blocks labelled SECOND LEVEL DECODER PLUS WORD DRIVERS, STORAGE, and SENSE AMPLIFIERS PLUS DATA BUFFERS correspond to Data Storage Logic Drawings. The block labelled BIT DRIVERS corresponds to Bit Driver Logic Drawing. The blocks labelled ADDRESS REGISTER, FIRST LEVEL DECODER, and TIMING AND CONTROL correspond to Memory Control Logic Drawing.

Detailed memory operation will be described for both the LOAD (Write) case and UNLOAD (Read) case. Reference to the three logic drawings will be made throughout the discussion.

To load data into one of the 128 addresses, the following sequence is followed. The LOAD signal is applied to the input of the two circuits shown on the Memory Control Logic Drawing. The output signal from one of the two circuits is DTS. The WCB signal from the Bit Driver Logic Drawing allows the selected word line to reach the write amplitude of +3V. The DTS signal turns on the 24 bit drivers. The second circuit generates two signals which are used as inputs to the ADDRESS REGISTER along with the ADDRESS INPUTS. The ADDRESS INPUTS (EAI) starting time coincides with the LOAD signal starting time.

The DATA INPUTS (EDI) start either at the same time as LOAD or 40 nanoseconds after LOAD, but end 120 nanoseconds after LOAD for both cases.

Depending on the level of the DATA INPUTS (EDI), the 24 bit drivers will either sit at the standby level (for "1" DATA) or go negative on the bit lines to -0.6V (for "0" DATA), when the DTS signal is applied. At the conclusion of this sequence, the appropriate binary one and zero pattern has been written into the selected address.

To unload data from one of the 128 addresses, the following sequence is followed. The ADDRESS INPUTS (EAI) and UNLOAD signals are applied. The X and Y signals are turned on. The appropriate word driver is then selected and its word line reaches the read amplitude level of +1.5V. Depending on the data stored in the storage bits of the selected address, the appropriate pattern appears on the 24 common bit sense lines after the word line has reached the read level. The amplitude of the signal appearing on the sense line is extremely low level: a one signal is +40mV and a zero is -20mV. The sense amplifier functions as an amplitude comparator as well as a linear amplifier. The signal on the sense line is compared in the amplifier with respect to ground. All signals above ground appear at the output of the sense amplifier at a +3V level. All signals below ground on the sense line appear at the output of the sense amplifier at -0.5V. The output of the sense amplifier drives the DATA BUFFERS from which the DATA OUTPUTS appear. At the conclusion of this sequence, the appropriate binary one and zero pattern has been unloaded from the selected address.

3-4 MicroCELL Assembly

The MicroCELL Memory System contains all functions, shown on Figure 2-1, on four printed circuit boards. The physical assembly of each of the four boards is shown on four assembly drawings which are related to logic drawings as follows:

The Data Storage Assembly Drawing corresponds to the Data Storage Logic Drawing. The Bit Driver Assembly Drawing corresponds to the Bit Driver Logic Drawing. The Memory Control Assembly Drawing corresponds to the Memory Control Logic Drawing. The negative TTL Output Interface Assembly Drawing corresponds to the negative TTL Interface Logic Drawing.

All components shown on Logic Diagrams are labelled and can be related to components on Assembly Diagrams.

3-5 MicroCELL Operation

The operation and characteristics of each function of the MicroCELL are described.

The circuit for 1 bit of the 16 bit storage device, DWSA, is shown in Figure 3-2. The storage of data is achieved by the flip-flop formed by transistors T_1 and T_2. A binary zero is stored in the bit when T_1 is ON and a binary one is stored when T_2 is ON. In essence, this storage is accomplished by moving node V_1 either negative (binary zero) or positive (binary one) with respect to GND. Node V_1 is moved by the proper polarity, amplitude, and timing of pulses on the WORD LINE and BIT-SENSE LINE through the gate transistor T_3. The pattern of pulses to write and read this storage bit is shown in Figure 2-3. The amplitudes of the pulses have been given in Paragraph 3-3. The constraints on the waveform amplitudes for proper circuit operations are as follows:

1. The minimum write level is sufficient to turn T_2 ON (W"1").

2. The maximum read level does not turn T_1 OFF or T_2 ON (R" 0").

3. The minimum read level is sufficient to give a readout (R"1").

4. The maximum level on the bit line does not disturb unselected words (W"0").

The circuit for the word driver plus second level decoder is shown in Figure 3-3. The word driver is selected when the X and Y inputs go negative (-0.5V) from the standby level (+2.5V). The output on the WORD LINE is determined by WCB. For a LOAD operation, WCB goes positive (+4V) and the WORD LINE goes positive to +3V. For an UNLOAD operation WCB stays at standby (+0.3V) and the WORD LINE goes positive to +1.5V from the standby level of -0.2V.

The sense amplifier is the commercially available linear IC, μA710C, and the input and output characteristics are described in Paragraph 3-3.

OPERATION INFORMATION

The READ BUFFERS are CTμL965. There are 4 single input, single output complementary gates in the 965 package. The input-output levels are standard CTμL.

The Bit Driver, First Level Decoder, WCB, and DTS circuits are shown in detail on the two Logic Drawings. All levels have been specified with the exception of DTS which is +2V standby and +0.3V ON.

VOLTAGE	COLOR CODE	PIN NUMBER	WIRE SIZE
13	GRAY	33	20
5	GREEN	1-5, 18-22 (Incl.)	20
2	RED	11-13 28-29 (Incl.)	20
-2	ORANGE	14-15 30-32 (Incl.)	20
-5	BLUE	6-10 23-27 (Incl.)	20
-1.6	BROWN	16,17	20
GROUND	BLACK	34-50 (Incl.)	20

LENGTH: 4 FEET

Figure 3-1 DETAILS OF POWER CABLE

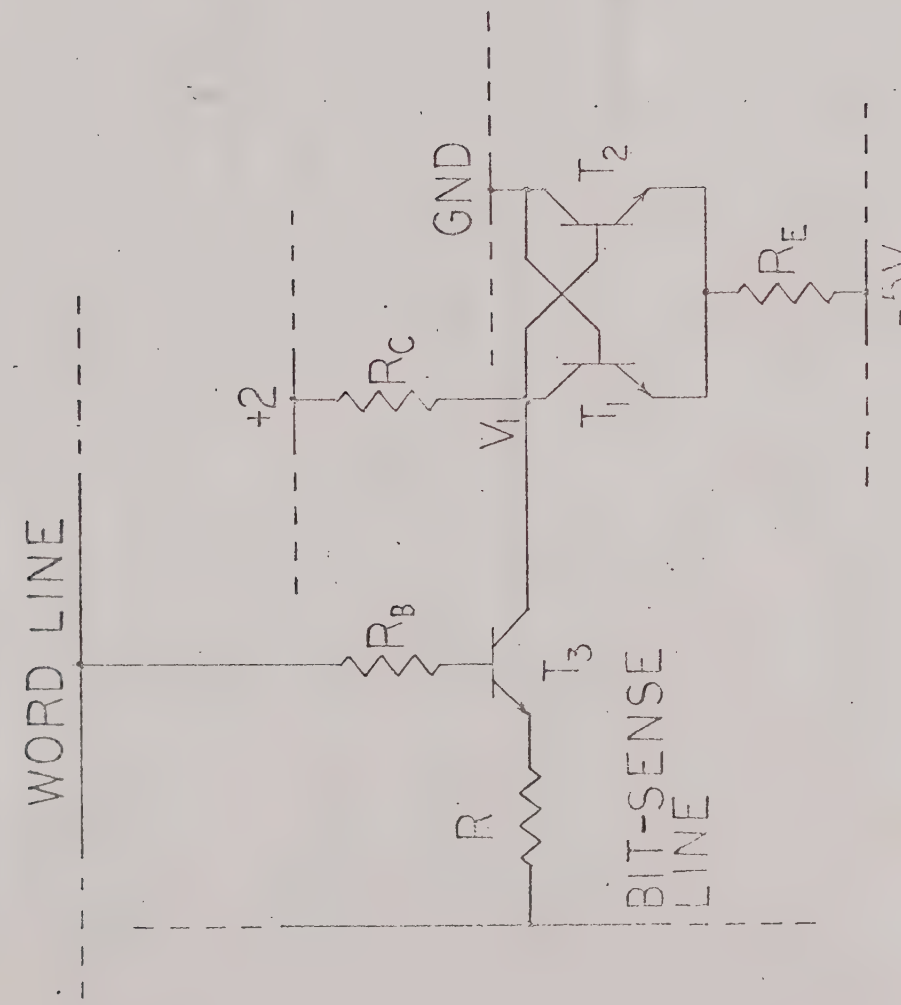

Figure 3-2 ONE BIT OF 16 BIT STORAGE DEVICE

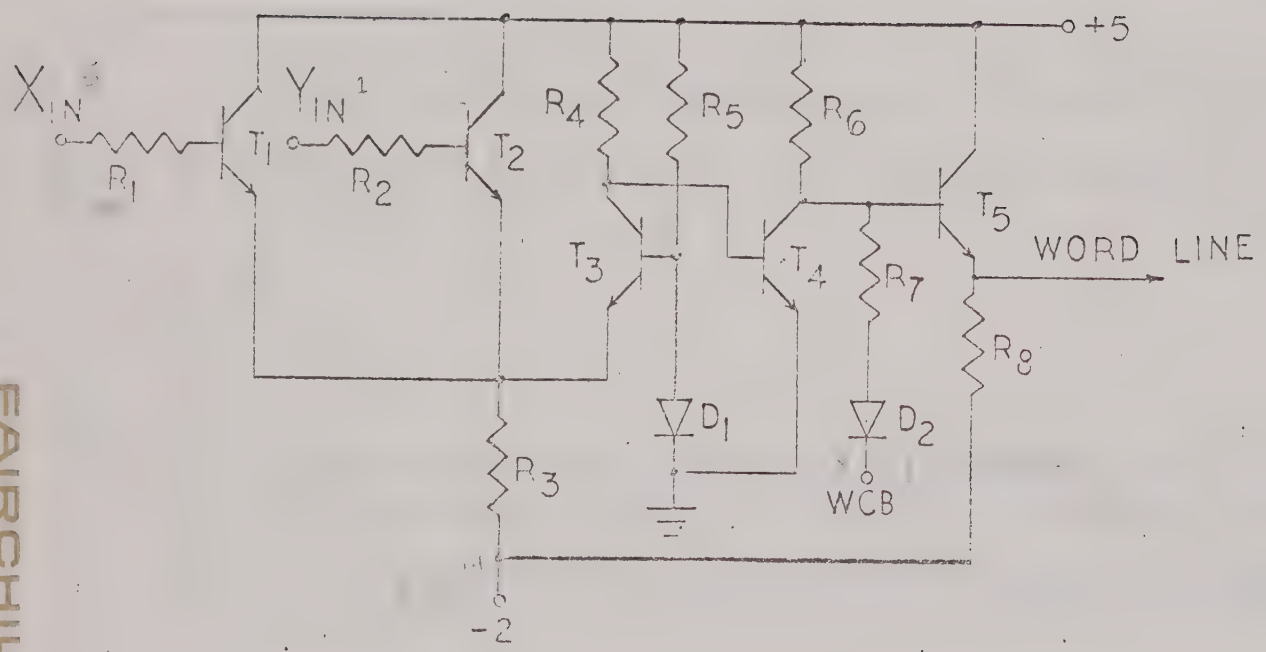

Figure 3-3 WORD DRIVER PLUS SECOND LEVEL DECODER

J8-1	EDI-1	J9-1	DO-1	J10-1	EAI-1
J8-2	GND	J9-2	GND	J10-2	GND
J8-3	EDI-2	J9-3	DO-2	J10-3	EAI-2
J8-4	GND	J9-4	GND	J10-4	GND
J8-5	EDI-3	J9-5	DO-3	J10-5	EAI-3
J8-6	GND	J9-6	GND	J10-6	GND
J8-7	EDI-4	J9-7	DO-4	J10-7	EAI-4
J8-8	GND	J9-8	GND	J10-8	GND
J8-9	EDI-5	J9-9	DO-5	J10-9	EAI-5
J8-10	GND	J9-10	GND	J10-10	GND
J8-11	EDI-6	J9-11	DO-6	J10-11	EAI-6
J8-12	GND	J9-12	GND	J10-12	GND
J8-13	EDI-7	J9-13	DO-7	J10-13	EAI-7
J8-14	GND	J9-14	GND	J10-14	GND
J8-15	EDI-8	J9-15	DO-8	J10-15	
J8-16	GND	J9-16	GND	J10-16	GND
J8-17	EDI-9	J9-17	DO-9	J10-17	EIL
J8-33	GND	J9-33	GND	J10-33	GND
J8-18	EDI-10	J9-18	DO-10	J10-18	EUL
J8-34	GND	J9-34	GND	J10-34	GND
J8-19	EDI-11	J9-19	DO-11	J10-19	
J8-20	GND	J9-20	GND	J10-20	GND
J8-21	EDI-12	J9-21	DO-12	J10-21	
J8-22	GND	J9-22	GND	J10-22	GND
J8-23	EDI-13	J9-23	DO-13	J10-23	
J8-24	GND	J9-24	GND	J10-24	GND
J8-25	EDI-14	J9-25	DO-14	J10-25	
J8-26	GND	J9-26	GND	J10-26	GND
J8-27	EDI-15	J9-27	DO-15	J10-27	
J8-28	GND	J9-28	GND	J10-28	GND
J8-29	EDI-16	J9-29	DO-16	J10-29	
J8-30	GND	J9-30	GND	J10-30	GND
J8-31	EDI-17	J9-31	DO-17	J10-31	
J8-32	GND	J9-32	GND	J10-32	GND
J8-35	EDI-18	J9-35	DO-18	J10-35	
J8-36	GND	J9-36	GND	J10-36	GND
J8-37	EDI-19	J9-37	DO-19	J10-37	
J8-38	GND	J9-38	GND	J10-38	GND
J8-39	EDI-20	J9-39	DO-20	J10-41	
J8-40	GND	J9-40	GND	J10-42	GND
J8-41	EDI-21	J9-41	DO-21	J10-43	
J8-42	GND	J9-42	GND	J10-44	GND
J8-43	EDI-22	J9-43	DO-22		
J8-44	GND	J9-44	GND		
J8-45	EDI-23	J9-45	DO-23		
J8-46	GND	J9-46	GND		
J8-47	EDI-24	J9-47	DO-24		
J8-48	GND	J9-48	GND		

NOTE: Pins J10-45 thru J10-50 on the MicroCELL Memory System are at +5V. Do not wire any lines from the CPU to these pins.

FIGURE 3-4 INTERFACE CONNECTOR CHART

OPERATIONAL INFORMATION

SIGNALS AND THEIR

DESCRIPTION

SIGNAL	DESCRIPTION
1. ELD	LOAD (Write Request)
2. LDI	LOAD INTERFACE. This signal would be different from ELD only in systems with input interface circuitry.
3. EUL	UNLOAD (Read Request)
4. WCB	WRITE CONTROL BUS. This signal allows the selected Word to reach the write amplitude.
5. DTS	DATA TRANSFER STROBE. This negative going signal turns on the Bit Drivers.
6. EDI	EXTERNAL DATA INPUT. These are the data signals going into the system.
7. DI	DATA INPUT. These are the input signals going into the storage multi-vibrators.
8. EAI	EXTERNAL ADDRESS INPUT.
9. X0,---,X15, Y0,---,Y15, Z0,---,Z3	These are the second level decoding signals.
10. A.$\bar{A}$,---,K,$\bar{K}$	These are the first level decoding signals.
11. DO	DATA OUTPUT.

Table 3-1

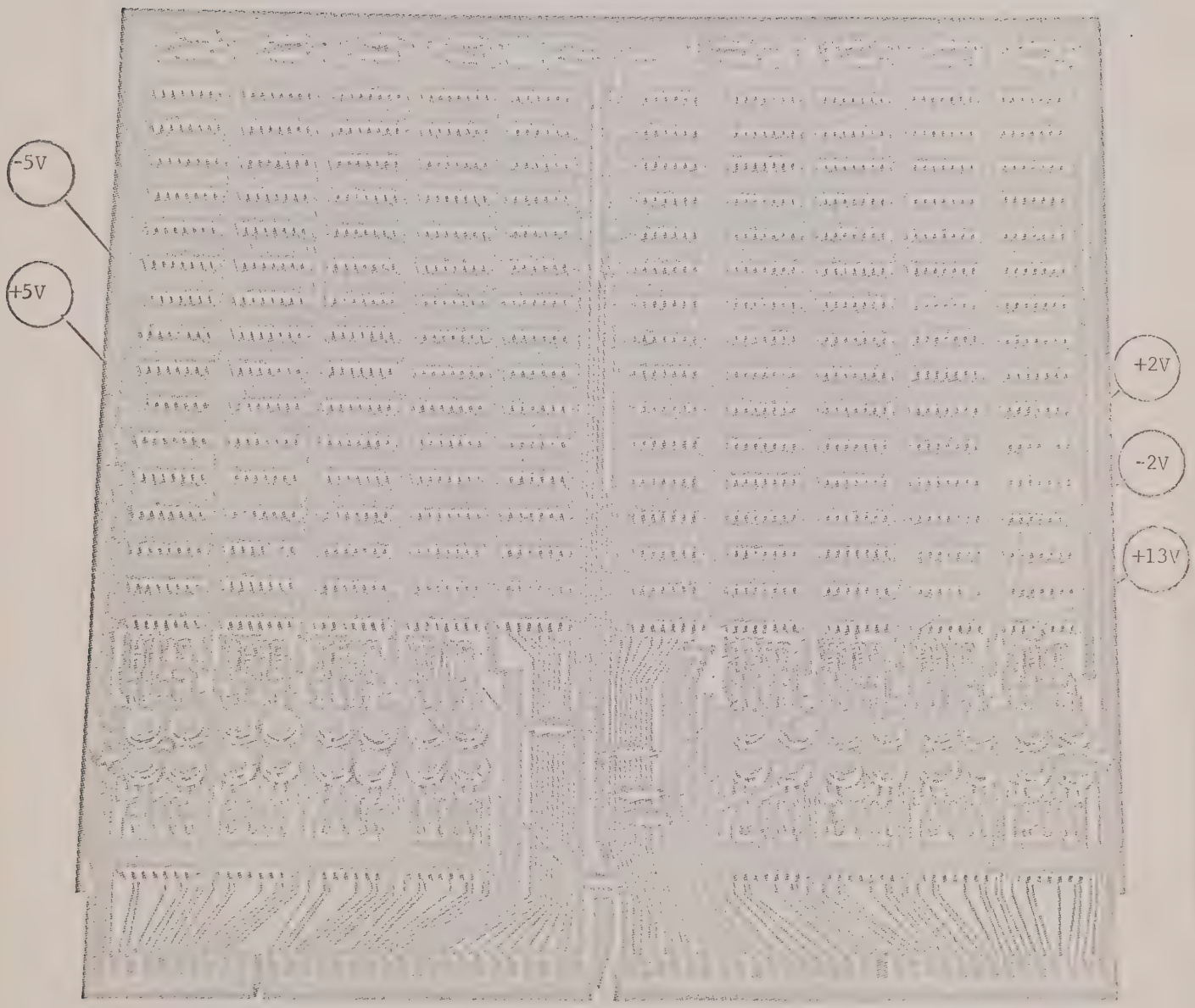

FIGURE 3-5 DATA STORAGE BOARD VOLTAGE CHECK POINTS

SECTION IV

MAINTENANCE PROCEDURES

4-1 Introduction

This section covers maintenance procedures to allow error free operation of the MicroCELL Memory System.

4-2 Maintenance

Table 4-1 lists error types with probable causes and solutions for each cause.

The following conditions are assumed to be normal and, therefore, would not be considered causes for failure.

1. All voltages are at the nominal values.

2. Overall system timing is correct.

TABLE 4-1 ERROR LIST

ERROR TYPES	PROBABLE CAUSES	SOLUTIONS
I-1 Failure to load one's during LOAD operation into all bits of one selected word.	I-1 Defective word driver. I-2 Improper X_{IN} or Y_{IN}.	I-1 Replace appropriate DWDA package. I-2 Check output of FIRST LEVEL DECODER
II-1 Failure to load one's during LOAD operation into all bits of all selected words.	II-1 WCB signal staying at the low level of +0.3V.	II-1 Check out WCB circuit.
III-1 Failure to load one's during LOAD operation into any bit of all selected word.	III-1 Appropriate bit line sitting at W"O" level,-0.5V, or more negative	III-1 Check out appropriate bit driver.
IV-1 Failure to load one's during LOAD operation into any bit of one selected word.	IV-1 Defective storage bit	IV-1 Replace appropriate DWSA package
V-1 Failure to unload one's during UNLOAD operation from any bits of any words where one's had been previously loaded during the LOAD operation	V-1 Bit driver timing problems. Leading or trailing edges of appropriate bit driver waveforms are out of spec (see Figure 3-2)	V-1 Check out appropriate bit driver.
VI-1 Failure to unload one's during UNLOAD operation from one bit of all words.	VI-1 Defective sense amplifier (CONTINUED)	VI-1 Replace appropriate μA710C.

TABLE 4-1 ERROR LIST
(CONTINUED)

ERROR TYPES	PROBABLE CAUSES	SOLUTIONS
VII-1 Failure to unload one's during UNLOAD operation from all bits of one word.	VII-1 Defective word driver. VII-2 Improper X_{IN} or Y_{IN}. VII-3 Word line resistor not making contact	VII-1 Replace appropriate DWDA package. VII-2 Check output of FIRST LEVEL DECODER VII-3 Solder word line resistor to appropriate word line.
VIII-1 Failure to unload one's during UNLOAD operation from one bit of one word	VIII-1 Defective storage bit.	VIII-1 Replace appropriate DWSA package.
IX-1 Failure to load zeros during LOAD operation into all bits of all words.	IX-1 WCB Signal staying at the high level of +4V IX-2 DTS Signal staying at the high level of +2V.	IX-1 Checkout WCB circuit IX-2 Checkout DTS circuit
X-1 Failure to load zeros during LOAD operation into one bit of all words	X-1 Defective bit driver	X-1 Replace appropriate bit driver.
XI-1 Failure to load zeros during LOAD operation into all bits of one word	XI-1 Defective word driver XI-2 Improper X_{IN} or Y_{IN} (CONTINUED)	XI-1 Replace appropriate DWDA XI-2 Check output of FIRST LEVEL DECODER

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MEMORY PRODUCTS

TABLE 4-1 ERROR LIST
(CONTINUED)

ERROR TYPES	PROBABLE CAUSES	SOLUTIONS
XII-1 Failure to load zeros during LOAD operation into one bit of one word	XII-1 Defective storage bit.	XII-1 Replace appropriate DWSA package
XIII-1 Failure to unload zeros during UNLOAD operation from one bit of all words	XIII-1 Defective Sense Amplifier	XIII-1 Replace appropriate μA710C
XIV-1 Failure to unload zeros during UNLOAD operation from all bits of one word.	XIV-1 Defective word driver	XIV-1 Replace appropriate DWDA
XV-1 Failure to unload zeros during UNLOAD operation from one bit of one word.	XV-1 Defective storage bit.	XV-1 Replace appropriate DWSA

SECTION V

POWER SUPPLY

5-1 Introduction

This section provides a description of the power supply used with the MicroCELL Memory System.

5-2 Description

The power supply provides the six voltages and currents listed in Table 1-1. The power supply regulates each voltage to the value shown in Table 1-1 using individual series regulators. Each voltage can be set using the individual potentiometers provided. Each potentiometer is identified by the voltage marked on the back panel over the appropriate hole. For further information on potentiometer locations, see Power Supply Installation Drawing.

The power supply serves four functions: raw power and rectification, logic, regulators, pass units.

Raw power and rectification circuitry is shown on Power Supply Circuit Diagram.

Logic circuitry is shown on Circuit Diagram Logic and Pass.

Regulator circuitry for all voltag values is shown on Circuit Diagram Regulator.

The pass unit circuitry is shown on Circuit Diagram Pass Board +5,-2.

The power supply includes a silicon controlled restifier (SCR) and a relay for over voltage protection. If any voltage tries to go more than 2 volts above its rated value, the SCR fires and opens the relay. This, in turn, pulls all six voltages to ground. The power supply must be switched OFF and then switched ON to restore all six voltages to their previous values.

SECTION VI

MISCELLANEOUS INFORMATION

6-1 Introduction

This section contains the following tables and drawings:

1. Accessories List
2. Figure 6-1 Component Pin Layout

6-2 Cannon Connector Information

The printed circuit boards are held in the Cannon connector by means of cam rods forcing contacts against the boards. The boards are inserted and withdrawn with the slots of the end caps in the vertical position. To lock the board in place after it has been inserted, the bottom end cap should be rotated in the clockwise direction and the end cap at the top of the board should be rotated counterclockwise. In the locked position, the slots of the end caps are horizontal. When the next higher board is locked, the top end cap now becomes the bottom end cap. It now must be rotated 180° in the clockwise position and end up with the slot horizontal. The end cap for this board must be rotated counterclockwise. This procedure continues for each higher board position. The top end cap is rotated clockwise and the bottom end cap counterclockwise to where the slot is in the vertical position.

NOTE: From the all boards locked position, the cam rods can only be rotated 90° clockwise or 90° counter-clockwise.

6-3 Off-Line Operation

To convert the MicroCELL Memory System from on-line to off-line operation the following procedure is to be followed:

1. Turn the MicroCELL Power Supply OFF.
2. Remove interface connectors P8, P9 and P10.
3. Connect Exerciser test cable to J8 and J10.
4. Set Clock Switch (S1, mounted on Interface Connecter Bracket) to the INT. position.

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SEMICONDUCTOR

5. Remove front panel from System including connectors P12 and P13.

6. Open cam locks for card slot A7 using cam tool. See Paragraph 6-2.

7. Remove Interface Board from card slot A7.

8. Insert Internal Exerciser Board into card slot A7. Close cam locks.

9. Replace front panel assembly. Connect P12 and P13.

10. Turn the MicroCELL Power Supply ON.

11. Set Mode Selected Switch to LOAD AND STOP position.

12. Set ERROR STOP/ERROR BYPASS Switch to ERROR STOP position.

13. Select a data pattern: "0", "1", "01" or "10".

14. Press and release RESET switch.

15. Press and release START switch.

16. Select a mode: UNLOAD ONLY, LOAD-UNLOAD ALT, UNLOAD-LOAD ALT, LOAD-UNLOAD.
    Note: Do not change data pattern without a load and stop operation of the data pattern that is to be checked.

17. Press and release RESET switch.

18. Press and release START switch.

    If there is an error the exerciser will stop two addresses past the faulty word.

    If there is no error the exerciser will continue to cycle.

19. To stop exerciser, press and release STOP switch.

    To check other data patterns, repeat steps 13-19.

    For a description of the exerciser's operational mode capabilities see Table 6-1.

    Table 6-2 lists the test capability of the exerciser.

MISCELLANEOUS INFORMATION

Accessories List

Offset Cam Tool (For End Caps)	1 Each
Slide Mounting Hardware	1 Bag
50 Pin Amphenol Interface Connector	3 Each
Power Supply Cable	1 Each
Exerciser Test Cable	1 Each
Technical Manual	2 Each

MODE	CAPABILITY
1. LOAD AND STOP	The exerciser cycles through all addresses for one pass loading any one of four data patterns and stops.
2. UNLOAD ONLY	The exerciser cycles through all addresses continuously unloading and error checking the contents of each address. The exerciser will stop two addresses past a word with the faulty information. The error bypass option is provided to allow the exerciser to free run despite the presence of faulty data.
3. LOAD AND UNLOAD ALTERNATE	The exerciser cycles through all addresses loading the preset data into odd words and unloading the previously stored data from even words. Error checking is provided during unloading only.
4. UNLOAD AND LOAD ALTERNATE	The exerciser cycles through all address unloading the previously stored data from odd words and loading the preset data into even words. Error checking is provided during unloading only.
5. LOAD AND UNLOAD	The exerciser cycles through all addresses loading the preset data into all words and then unloading the data from these words. Error checking is provided during unloading only.

Table 6-1 Exerciser Operational Mode Capabilities

CONDITIONS TESTED	EXERCISER SET-UP AND PROCEDURE
1. "1" Storage in all words	(a) Set Mode switch to LOAD AND STOP. (b) Set Data to "1". (c) Reset exerciser. (d) Push start button. (e) Set Mode switch to UNLOAD only. (f) Push Reset button. (g) Push Start button.
2. "0" Storage in all words	(a) Same procedure as condition (1) except for stop (b) where Data is set to "0" instead of "1".
3. Bit line recovery and minimum "1" signal readout	(a) Set Mode switch to LOAD and STOP. (b) Set Data to "1" (c) Reset exerciser. (d) Push Start button. (e) Set Mode switch to LOAD and UNLOAD ALTERNATE. (f) Set Data to "01" pattern (g) Push Reset button. (h) Push Start button. NOTE: This set-up tests the bit line recovery at all odd word times and the minimum "1" signal readout for all even words. To checkout these other cases; that is, bit line recovery at all even word times and minimum "1" signal readout for all odd words, change only: (e) Set Mode switch to UNLOAD and LOAD ALTERNATE (f) Set Data to "10" pattern
4. Minimum word line write pulse, word line recovery time, and maximum "0" signal readout.	(a) Set Mode switch to LOAD and STOP. (b) Set Data to "0". (c) Reset exerciser. (d) Push Start button. (e) Set Mode switch to LOAD and UNLOAD ALTERNATE. (f) Set Data to "10" pattern. (g) Push Reset button. (h) Push Start button.

Table 6-2 Test Capability of the Exerciser.

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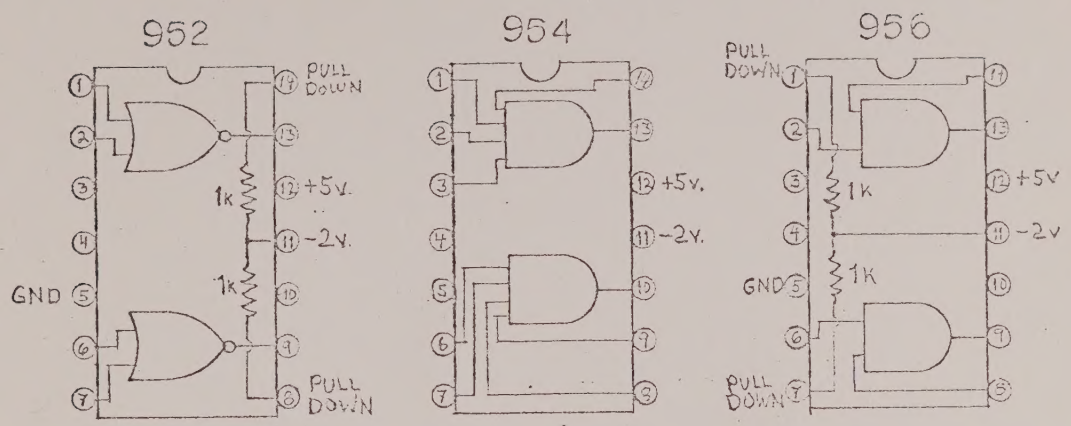
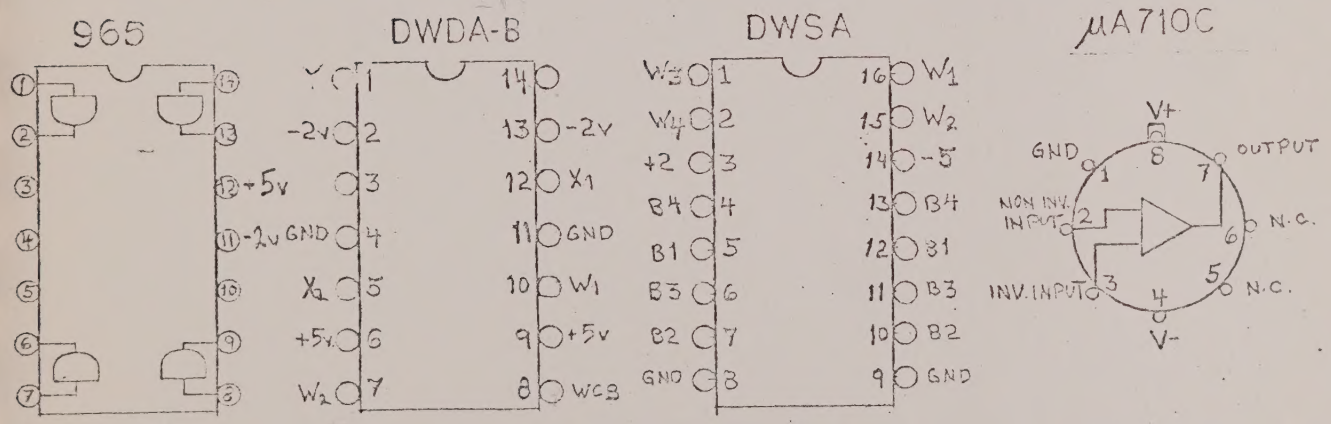
CONDITIONS TESTED		EXERCISER SET-UP AND PROCEDURE
4. Continued		NOTE: This set-up tests the minimum word line write pulse and word line recovery at all odd word times and the maximum "0" signal readout for all even words. To check the opposite condition change only: (e) Set Mode switch to UNLOAD and LOAD ALTERNATE. (f) Set Data to "01" pattern.
5. Maximum writing rate.	(a) (b) (c) (d)	Set Mode switch to LOAD and UNLOAD. Set Data to "10" pattern. Reset exerciser. Push Start button. NOTE: This set-up tests the maximum writing rate by alternating data in each word. For this case, all odd words will be loaded with "1"'s and all even words are loaded with "0"'s. When all words are loaded with the appropriate data, unloading of all words commences. Error checking is used to insure all words had the correct data loaded. To load all odd words with "0"'s and all even words with "1"'s. (b) Should be set to Set Data to "01" pattern.

Table 6-2 (continued)





W: WORD
B: BIT
WCB: WRITE CONTROL BUS

Figure 6-1 COMPONENT PIN DIAGRAM (TOP VIEW)

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